# **Comp. Arc. & Org** mid-term revision 2016

By

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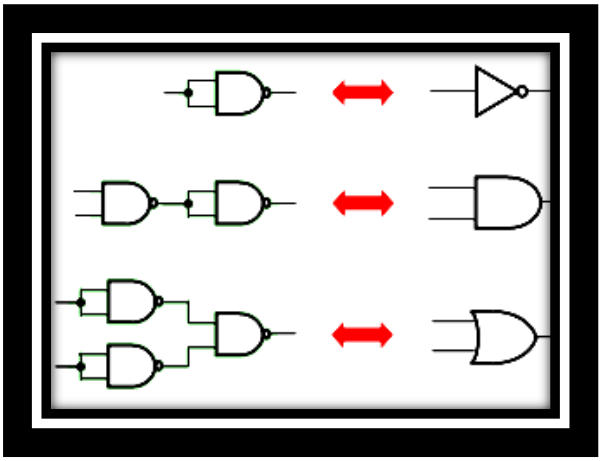
تعليمات عامة **بخصوص امتحان مادة معمارية وتنظيم الحاسبات** (**Comp. Arc. & Org**)

- امتحان منتصف الفصل الدراسي (الميدتيرم) مدته ساعة
- الحل في نفس ورقة الإمتحان **!!** وبمجرد استلامها تأكد من كتابة اسمك ومجموعتك/السكشن**!!**
- ممنوع تماما إحضار أي أوراق سواء تتعلق بالمادة أو لا ، وإلا اعتبر ذلك شروعا في الغش
- ممنوع إحضار أي أدوات سواء آلة حاسبة أو غيرها ، فقط القلم
- الإمتحان من ٢٠ درجة ، في أربع أسئلة
- هناك عدة نماذج امتحان ، وبالنسبة للفرقة الثانية هناك أسئلة لمجموعة أ غير أسئلة مجموعة ب
- بالنسبة للفرقة الثانية يفضل تخصيص مدرجي ١ و٢ للمجموعة أ ، وغير ذلك لمجموعة ب

# Chapter 1

## Q1 proof Universality of NAND

Answer



## Q2 complete

i. NAND also known as ….
ii. NOR also known as ….
iii. Sum-of-Product also known as ….

Answer

i. NAND also known as **Sheffer stroke**
ii. NOR also known as **Peirce arrow**
iii. Sum-of-Product also known as **conjunctive normal form (CNF)**

## Q3 True or false?

i. Combinational circuits have the ability to store information.
ii. The effect of arithmetic shift to the left is multiplying by 2
iii. Relation between fan-in and gate delay is quadratic

Answer

i. False
ii. True
iii. True

**Q1 Represent $21.75_{dec}$ in Floating point. Use the IEEE 754 standard**

21.75 in binary is 10101.11 or $1.010111\ 2^4$

S=0, Bias is $2^7$-1=127 E= 127 + 4 = 131

| 1bit | 8 bits | 23 bits |
|---|---|---|
| 0 | 10000011 | 01011100000000000000000 |

**Q2 Represent $-0.4375_{dec}$ in floating point, using IEEE standard 754**

Binary equivalent of –0.4375 = -.0111 or – $1.11\ 2^{-2}$

S= 1, Exponent is –2 + 127 =125 or 01111101

| 1bit | 8 bits | 23 bits |
|---|---|---|
| 1 | 01111101 | 11000000000000000000000 |

Q3 complete

i. Little-endian computers include ….
ii. ‘A’ is represented as … in ASCII
iii. ‘a’ is represented as … in ASCII
iv. ‘1’ is represented as … in ASCII

Answer

i. Little-endian computers include **Intel Pentium**
ii. ‘A’ is represented as ‘**100**0001’ (65 in decimal) in ASCII
iii. ‘a’ is represented as ‘**110**0001’ (90 in decimal) in ASCII
iv. ‘1’ is represented as ‘**011**0001’ (49 in decimal) in ASCII

Chapter 3

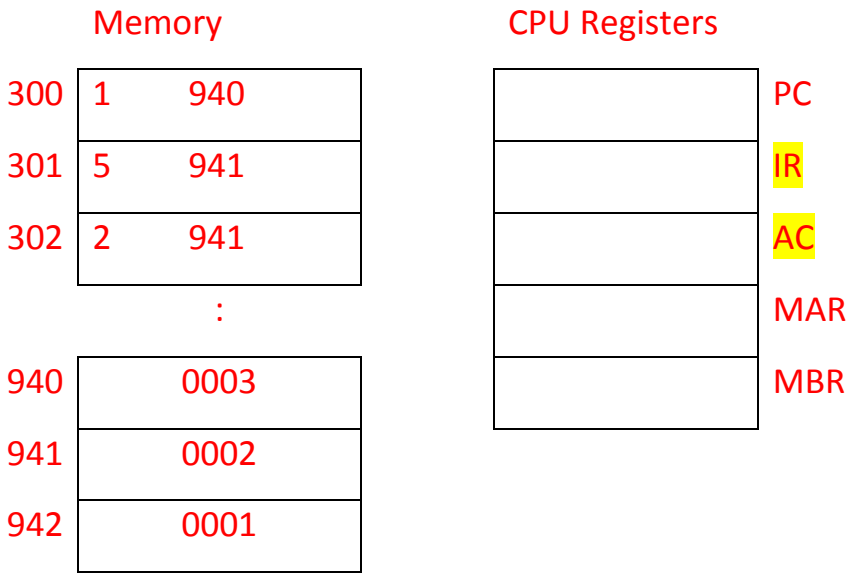
Q1 complete

i. **1st generation** of computer is based on …..
ii. The first electronic digital computer **is …..**
iii. **2nd generation** of computer is based on …

Answer

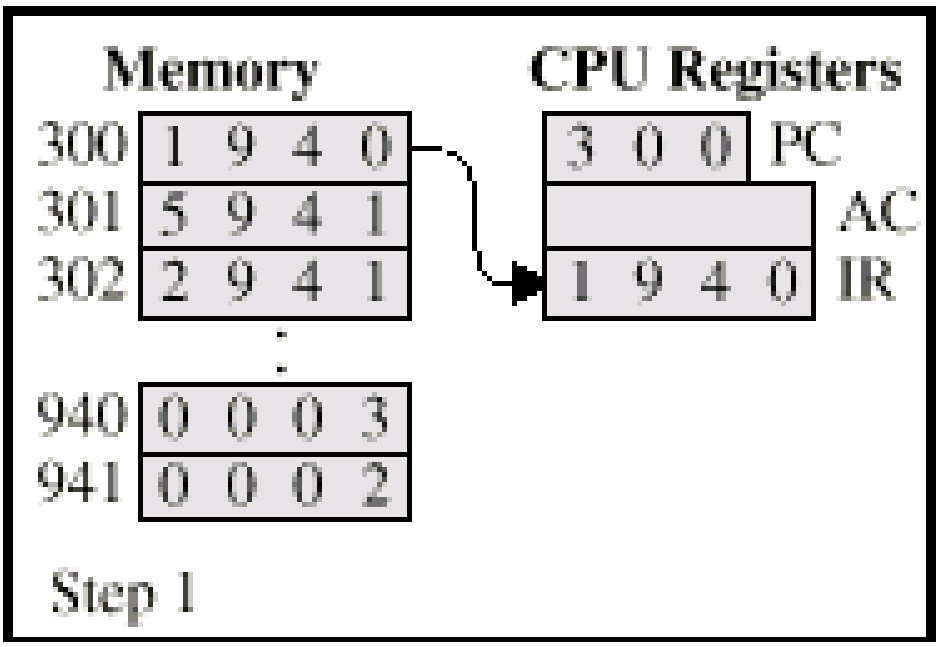
i. **1st generation** of computer is based on vacuum tubes.
ii. the first electronic digital computer **is Electronic Numerical Integrator And Computer (ENIAC)**
iii. **2nd generation** of computer is based on transistors.

Q2 Trace the Program Execution (**Op-Codes**: 1=load, 2=store, 5=add, …)

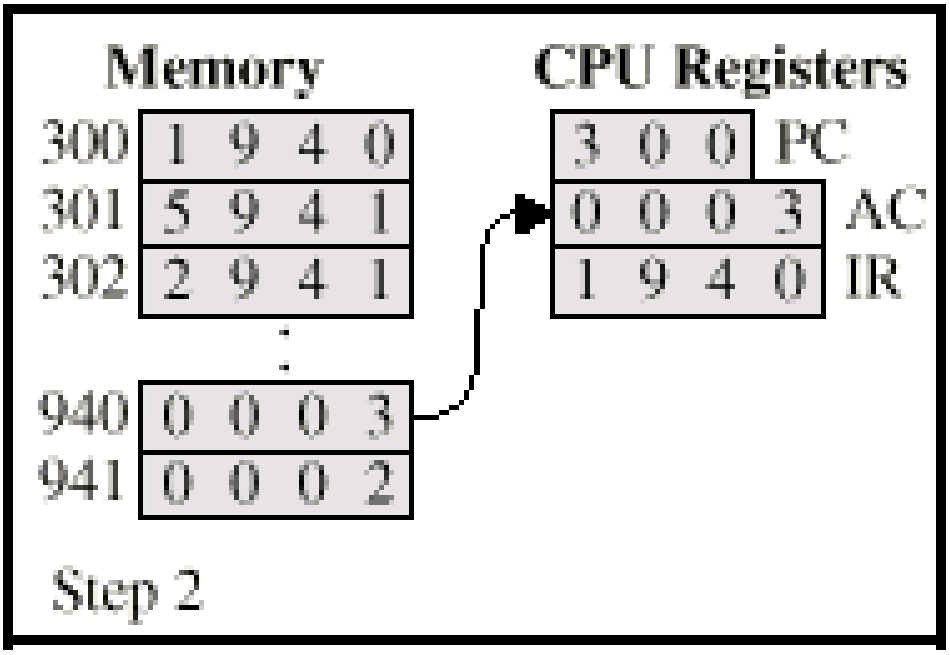


Answer :

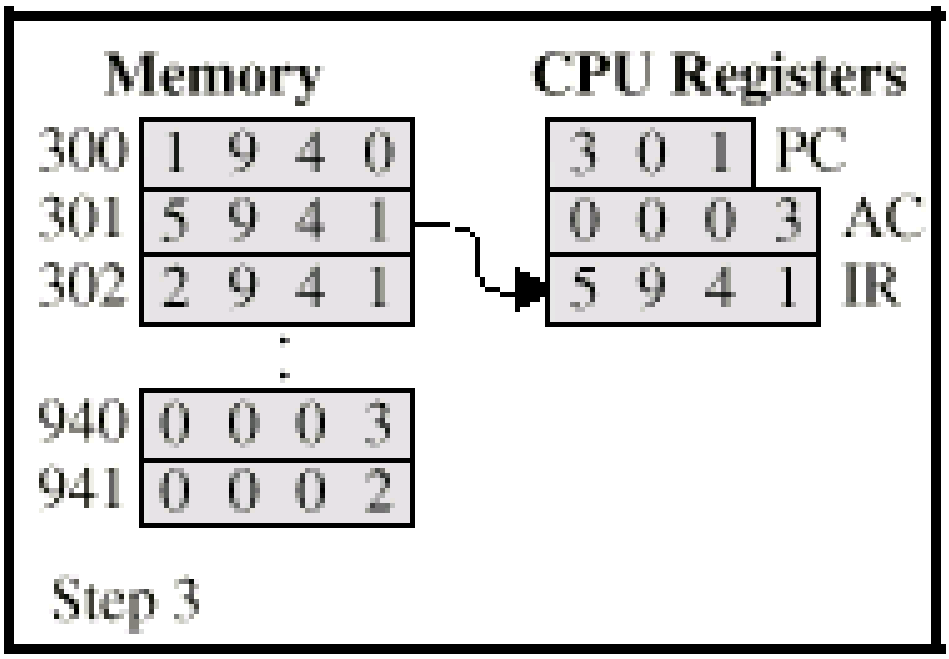
FETCH



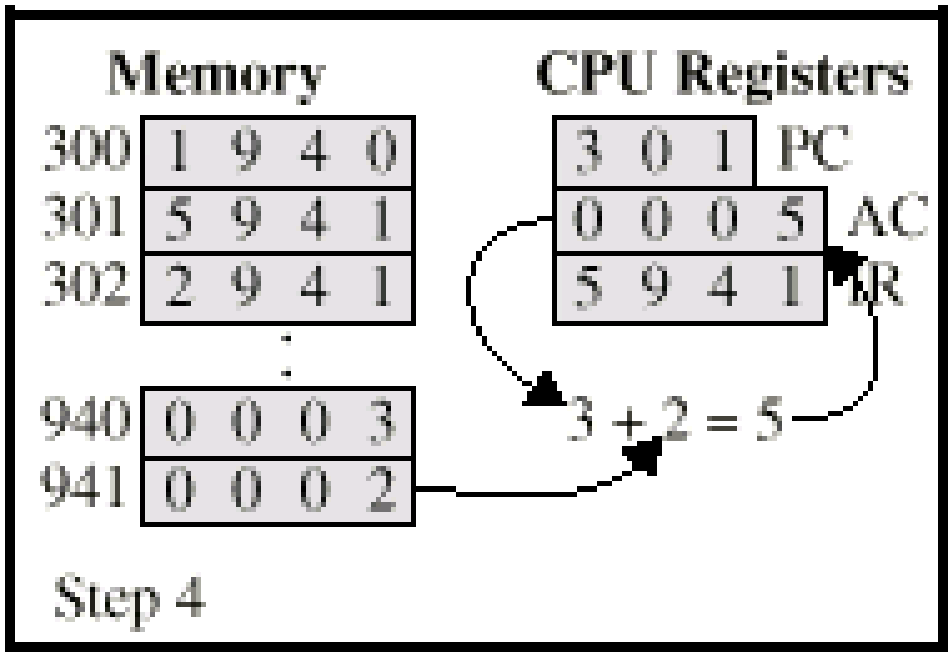

EXECUTE



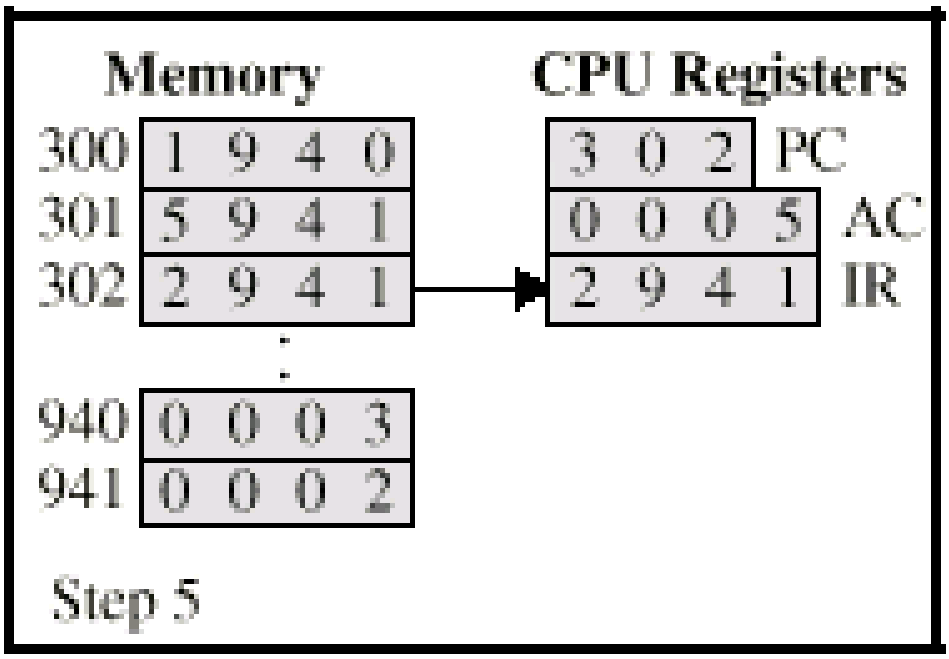
FETCH



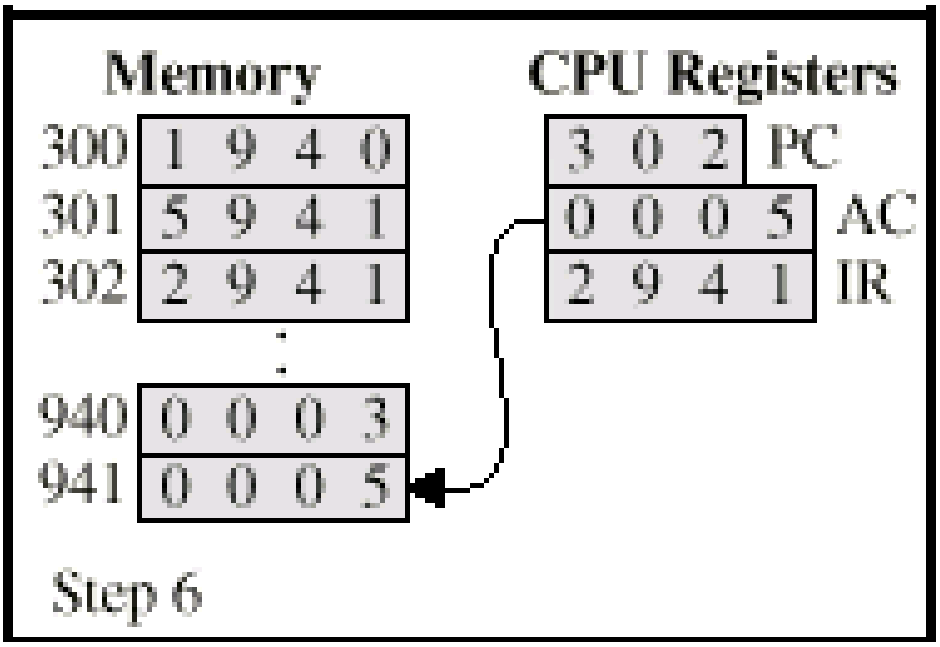

EXECUTE



FETCH




EXECUTE



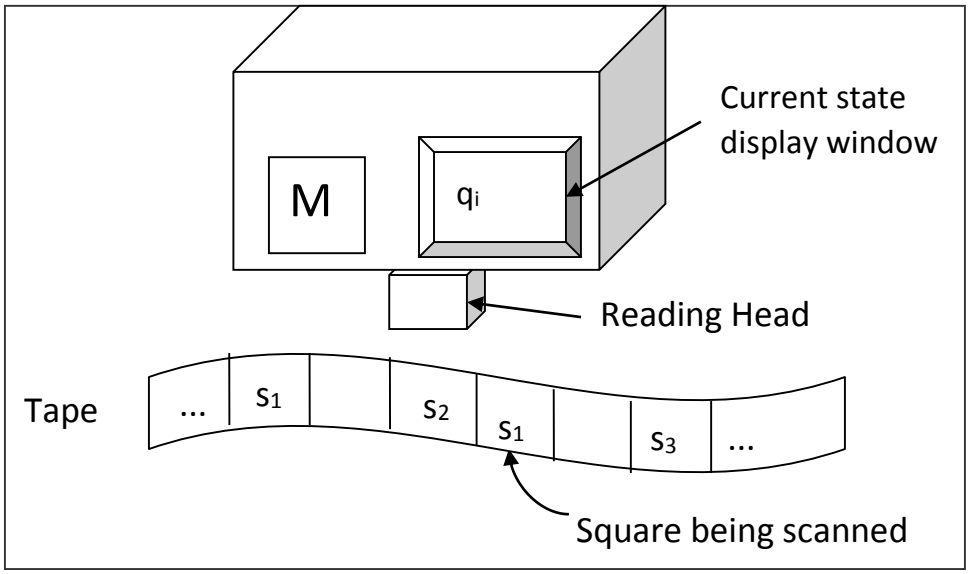
Q3 **Write full assembly program to print the ASCII Table**

```
.Model  Small
.Stack   100h
.Code
MAIN    PROC
        MOV AH , 2
        MOV  CX , 256
        MOV  DL , 0
Print_Loop:
        INT    21h              ;DL  اطبع الحرف الموجود في
        INC    DL               ; تجهيز الحرف التالي
        DEC    CX               ; انقص العداد
        JNZ    PRINT_LOOP       ;
; DOS_EXIT
        MOV  AH , 4Ch
        INT    21h
MAIN    ENDP
END     MAIN
```

سؤال لمجموعة أ

**Draw the architecture of Turing Machine**

.




سؤال لمجموعة أ

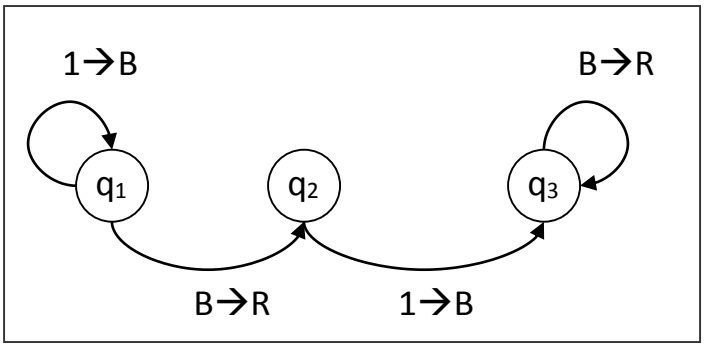
**Analyze output of the following Turing machine specification**

**$q_1$ 1 B $q_1$**
**$q_1$ B R $q_2$**
**$q_2$ 1 B $q_3$**
**$q_3$ B R $q_3$**

Initially, the tape contains x+y+2 occurrence of 1. This machine computes **x + y**.

The machine is designed just to erase two of these ones from left.

Here is a **state machine** showing addition on a Turing machine.



## سؤال لمجموعة ب

**Analyze output of the following program**

**$I_0$: input (x,y)**

**$I_1$: J(2, 3, 6)**

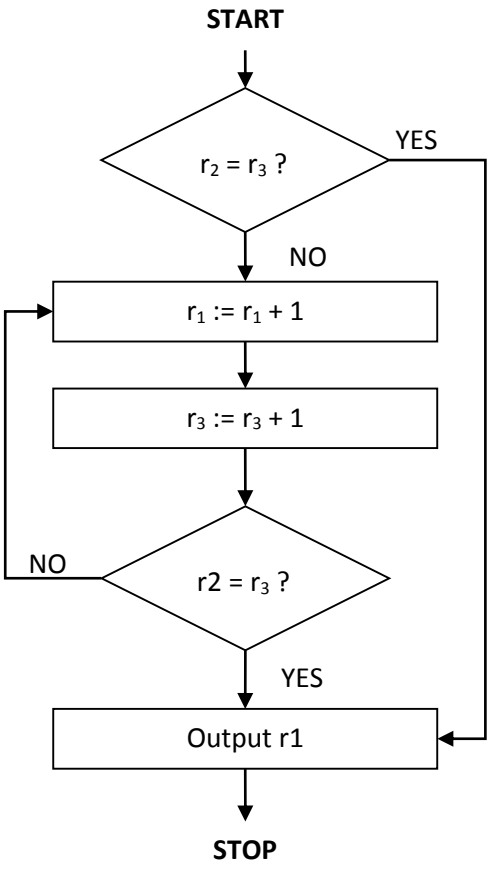
**$I_2$: S(1)**

**$I_3$: S(3)**

**$I_4$: J(2, 3, 6)**

**$I_5$: J(1, 1, 2)**

**$I_6$: output**




Initial Configuration

| x | y | 0 | |
|---|---|---|---|

After k cycles round the loop

| x+k | y | k | |
|---|---|---|---|

If y = k, output = x+y:

| x+k | y | k |
|---|---|---|

## سؤال لمجموعة ب

**Analyze output of the following program**

**$I_0$: input (x,y)**

**$I_1$: J(1, 2, 6)**

**$I_2$: S(2)**

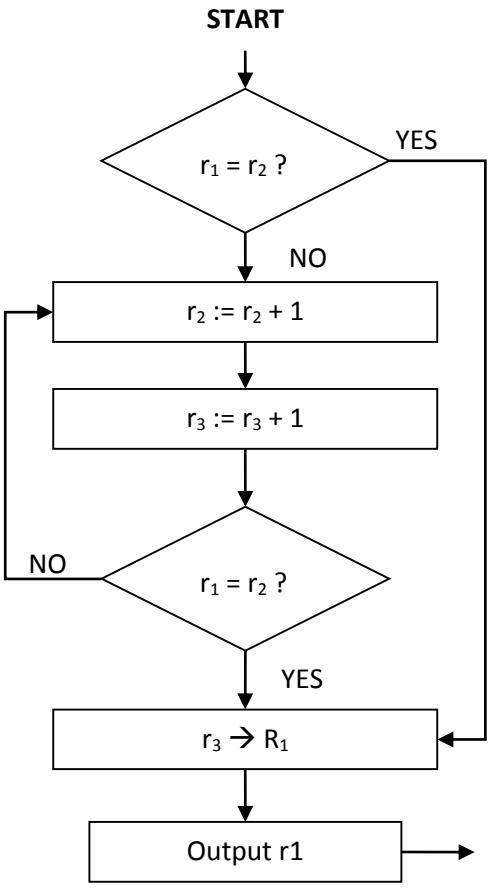
**$I_3$: S(3)**

**$I_4$: J(1, 2, 6)**

**$I_5$: J(1, 1, 2)**

**$I_6$: T(3, 1)**

**$I_7$: output**




Initial Configuration

| x | y | 0 | |
|---|---|---|---|

After k cycles round the loop

| x | y+k | k | |
|---|---|---|---|

If x = y+k, output = k=x-y

| k | y+k | k | |
|---|---|---|---|

سؤال للبرنامج المميز (هندسة البرمجيات) والدبلومات

**Convert the following C++ code segments into equivalent Assembly**

**a) for( r = 0; r < n; r++) { for_body }**

**b) if( x==y ){if_body} else {else_body}**

**c) int i ; do{ do_body } while(i != 5);**


Answer

**أجب بنفسك**

# Chapter 4

**Q1 complete**

i. …. it is the time between the instant that the memory address is stable in the MAR and the data are available in the MBR.
ii. Static RAM (SRAM) is a memory technology based on ….
iii. Dynamic RAM (DRAM) is a memory technology based on ….
iv. …is a mechanism for translating **logical** into physical **memory addresses**
v. Divide **physical** memory into fixed-sized blocks called ….
vi. Divide **logical** memory into blocks of same size called….

Answer

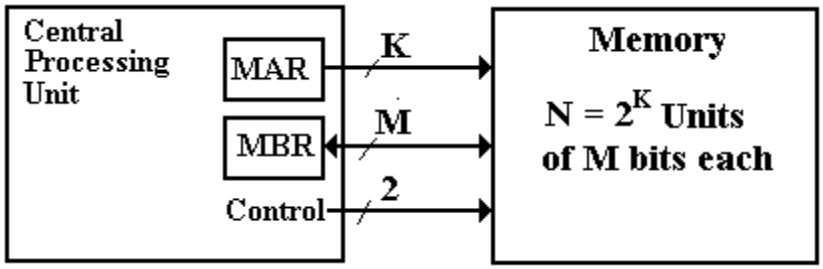
i. Memory access time
ii. flip-flops
iii. capacitors
iv. Virtual memory
v. **Frames**
vi. **pages**

**Q2Design 4GB byte-addressable memory showing length of MAR (K) & MBR (M)?**

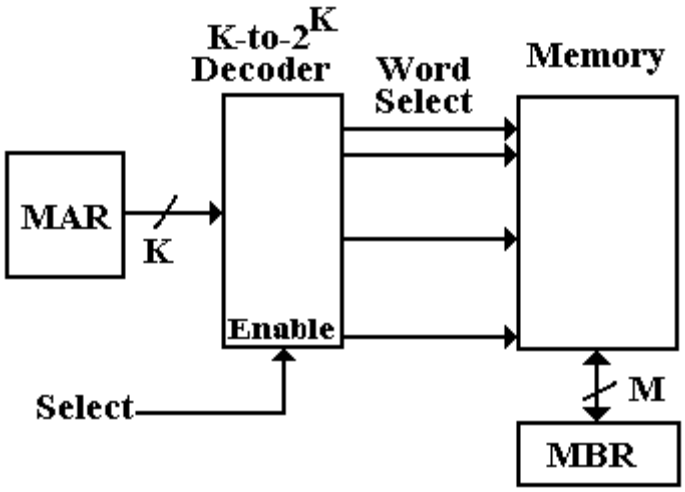
**Or Design 1MB byte-addressable memory showing the length of K and M?**

**Answer**

**Monolithic view** of the memory



The **linear view**



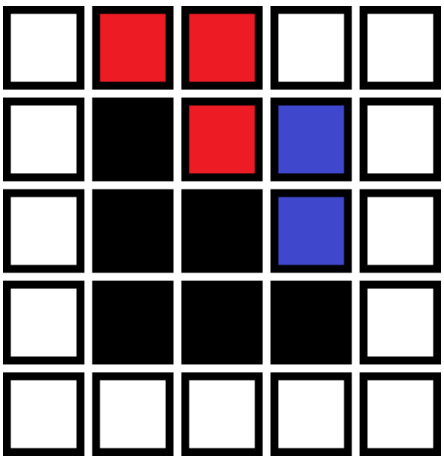

M= 8 bits

- A 1MB memory would use a 20–to–1,048,576 decoder, as $2^{20}$ = 1,048,576. ➔ K=20 bits
- A 4GB memory would use a 32–to–4,294,967,296 decoder, as $2^{32}$ ➔ K=32 bits

KB= $2^{10}$, MB= $2^{20}$, GB=$2^{30}$ ,

4GB= $4\times2^{30} = 2^2\times2^{30} = 2^{32}$

**Q3 Compress the following** 5×5 raster image (8-bit) using Boolean Logic and using Huffman Coding

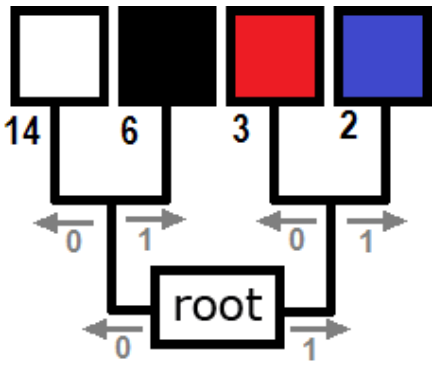


Answer

The uncompressed image will take 5 x 5 x 8 = 200 bits of storage.

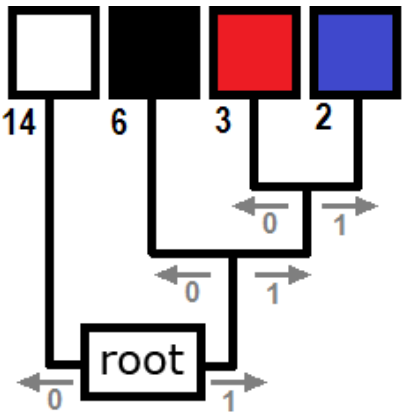
Decreasing frequency:


Binary tree (Boolean Logic) and corresponding code




| color | freq. | bit code |
|---|---|---|
| | 14 | 00 |
| | 6 | 01 |
| | 3 | 10 |
| | 2 | 11 |

Huffman tree and corresponding code




| color | freq. | bit code |
|---|---|---|
| | 14 | 0 |
| | 6 | 10 |
| | 3 | 110 |
| | 2 | 111 |

200-bit image compressed to 14 x 1 + 6 x 2 + 3 x 3 + 2 x 3 = 41 bits

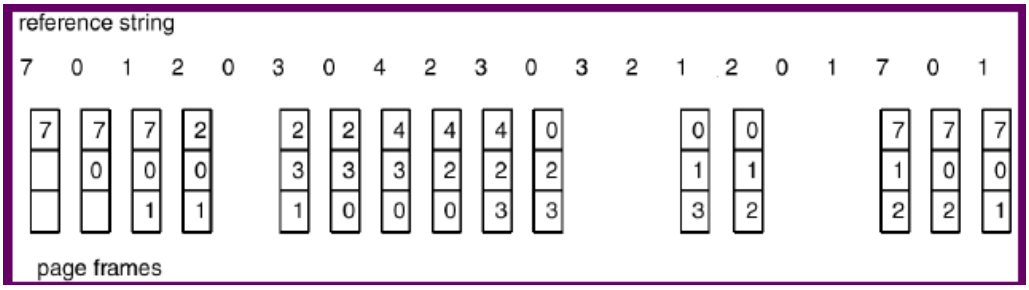
سؤال للبرنامج المميز (هندسة البرمجيات) والدبلومات

**Apply FIFO, Optimal, and LRU for 3 frames and the following reference string**

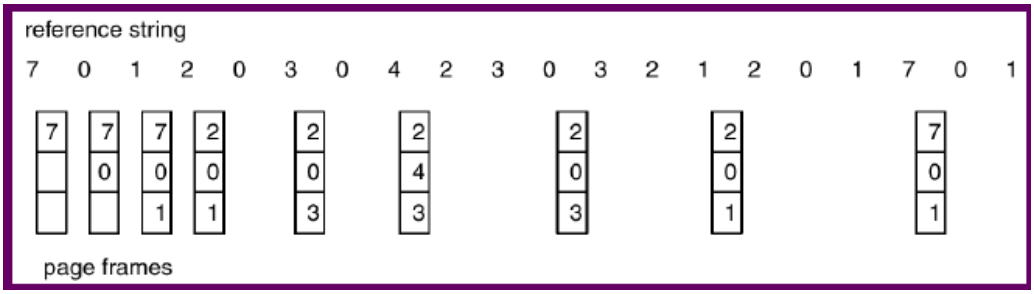
**7 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 7 0 1**

**Answer**

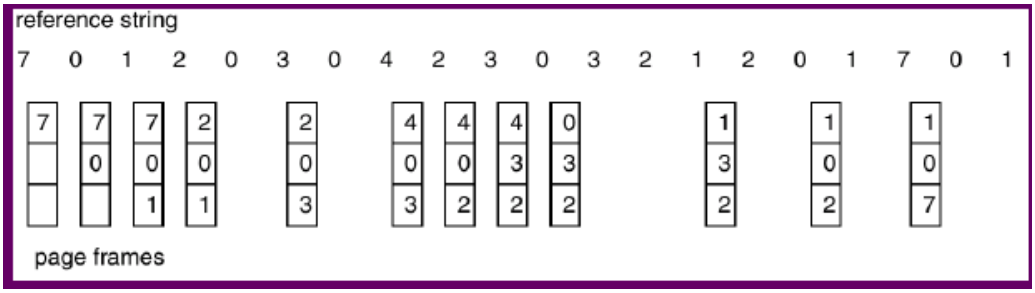
## First-In-First-Out (FIFO) Algorithm




## Optimal Algorithm

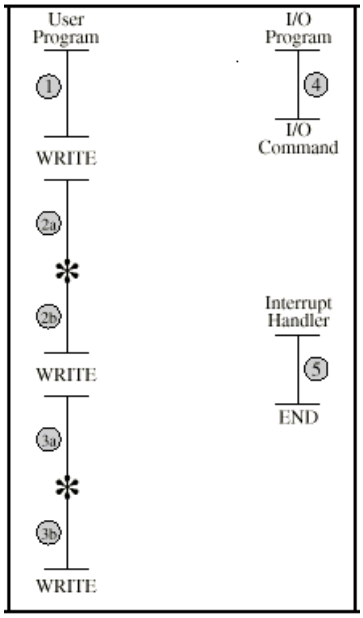



## Least Recently Used (LRU)

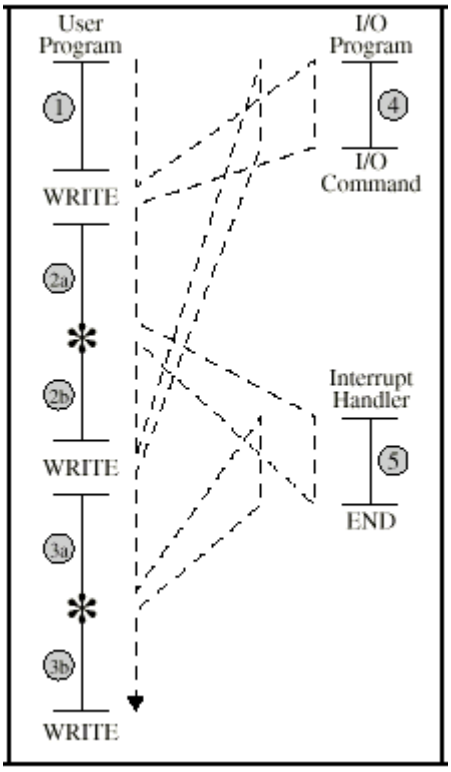


## Chapter 5

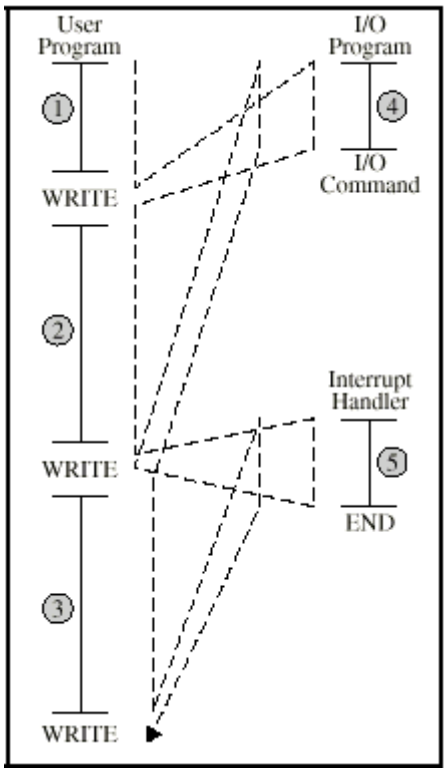
Q1: compare between short IO wait and long IO wait, by drawing a line that shows the execution path




Answer




Interrupt: short IO wait




Interrupt: long IO wait

## Q2 Complete

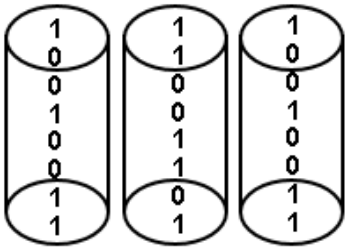
i. Independent bus request lines configuration is used in … bus
ii. Distributed Arbitration is used in …. bus

**Answer**

**Independent bus request lines** configuration is used in PCI bus.

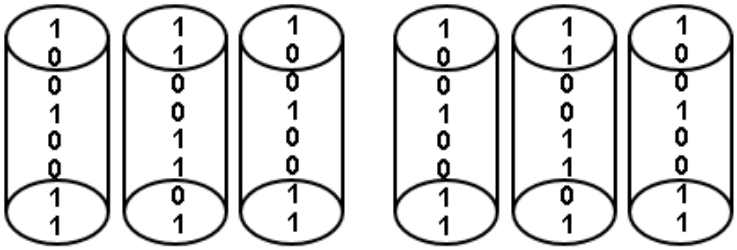
**Distributed Arbitration is** used in SCSI bus

## Q3 Apply RAID1 and RAID3 on the following data



Answer

**RAID1**



**RAID3**